Data Sheet

VIAVI Solutions

VIAVI

Xgig 16-lane Exerciser/Analyzer

for PCI Express® 6.0

The PCIe Exerciser/Analyzer generates PCIe 6.0 data streams and responses for in-depth testing and analysis at 64GT/s.

The VIAVI Xgig® PCIe 6.0 Exerciser/Analyzer, the 6P16, brings the next generation of high-speed 64 GT/s test capability to the Xgig PCIe product portfolio. The Exerciser is a valuable tool for debugging difficult protocol communication problems because it provides full, bit-level, repeatable control for generated PCIe 6.0, CXL and NVMe data traffic. The Analyzer allows detailed view of traffic between a host and endpoint device, supporting PCIe FLIT Mode, Non-Flit Mode, CXL, and NVMe.

The Exerciser generates PCIe complaint traffic and can be configured to emulate the operation of a Root Complex (RC or host system) or an Endpoint (EP) device. Ordered Sets (TS0, TS1, TS2, etc.), and TLP, DLLP, and LTSSM sequences can be defined, transmitted, and even modified in real-time based on user configuration.

The 6P16 Exerciser enables detailed validation and debug of the state machine of a PCIe 6.0 controller. It can provide insights for performance tuning of firmware and application software. The 6P16 can be programmed to generate non-compliant PCIe sequences to enable testing of boundary and stress conditions that are not normal to correct system operation and would otherwise be very difficult to evaluate.

The 6P16 Exerciser works in tight association with the Analyzer function to allow capture and decoding of complex test scenarios. Bidirectional captures can be saved for detailed analysis using VIAVI tools such as Expert™.

A scripting API is available so that complex, custom Exerciser test scripts can be created; either as original or modified from pre-defined library scripts.

The VIAVI PCIe 6.0 6P16 Exerciser/Analyzer Solution is a comprehensive solution with Exerciser and Analyzer functionality provided via a multi-function chassis and application-specific Analyzer or Exerciser Interposers.

Key Features

- Generates and responds to PCIe 6.0 64GT/s traffic
- Operates at 64GT/s PAM4, and supports all other PCIe data rates of 2.5, 5.0, 8.0, 16, and 32GT/s NRZ
- Supports links of 1, 2, 4, 8 and 16-lanes
- 64GB total memory (32GB to capture upstream and 32GB to capture downstream)
- User can set Exerciser link rates and widths and control transitions to other rates
- Fully integrated Analyzer/Exerciser enables a variety of test conditions
- Analyzer/Exerciser supports new PCIe FLIT Mode, FEC and TS0 Ordered Set
- Exerciser can create unique LTSSM test conditions via user customized branching
- LTSSM state tracker with history log
- User can define and save custom test configurations
- Versatile scripting API allows user to create custom test configurations for positive and negative test cases
- Scripting API allows creation of complex, user-defined test cases
- Powerful graphical control interface provides quick status information and fast setup of test cases
- Xgig Analyzer/Exerciser tools operate on a Windows enabled PC

Xgig Exerciser Interface – Start Page

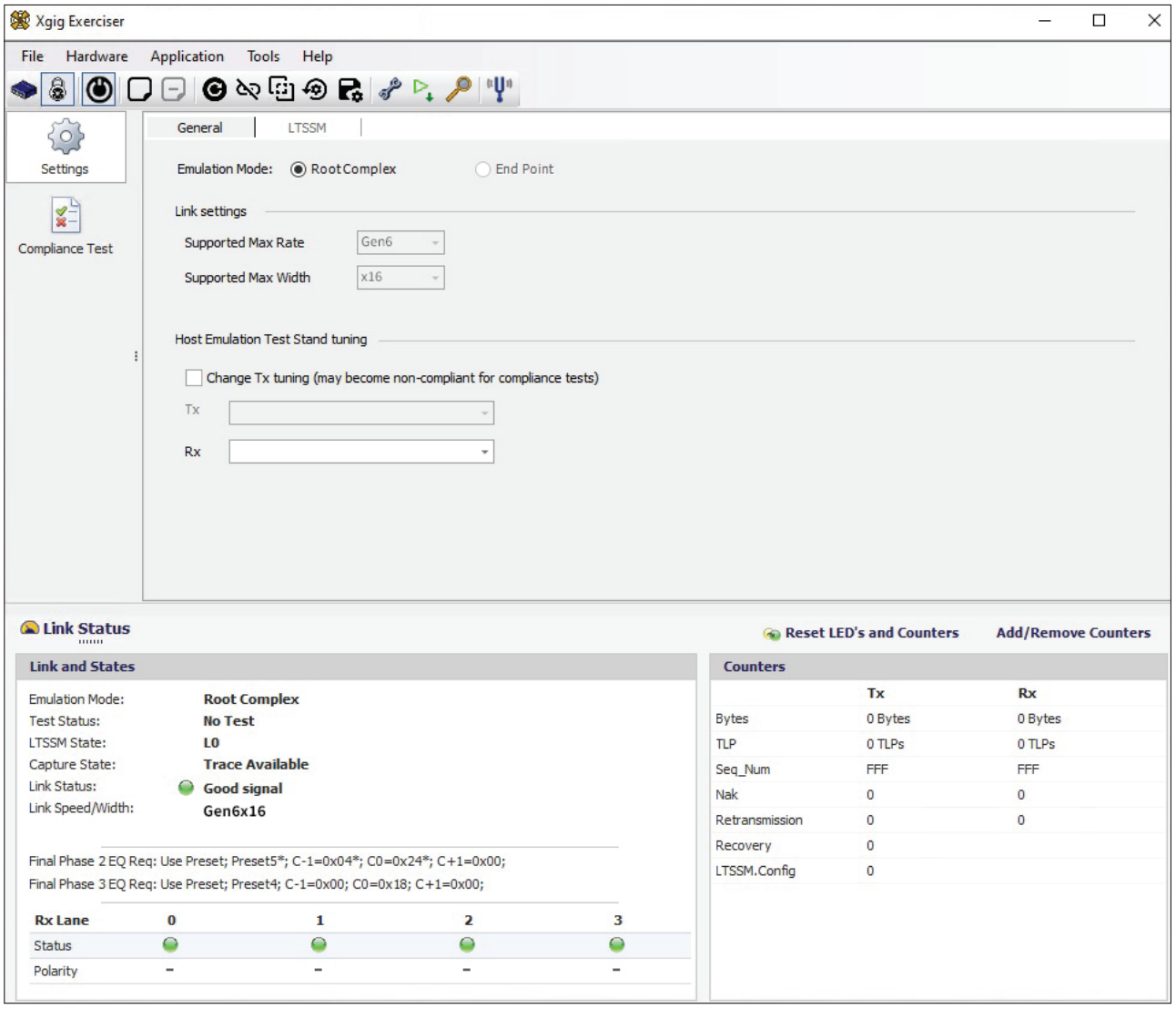

Figure 1 – Exerciser Start Screen

Exerciser User Interface

The Xgig PCIe Exerciser user interface makes it easy to set up and execute a test. Figure 1 above shows the Exerciser launch screen. The top bar includes the typical Windows™ control items. The second bar down has various quick launch buttons for tasks done often.

On the left side are icons for Settings, Compliance Tests, and other features. The Settings>General tab is the first that is presented. Information on the test bench configuration is provided including clocking, reset and other basic controls.

From Settings, controls for the extensive Exerciser parameters are accessible. The LTSSM tab provides control over link settings and operation.

For example, TX and RX setting can be adjusted from this tab. It also allows setting timeouts and other parameters. The Settings tab allows forcing limits on the test data rate and maximum link width.

Below the Settings icon, the Compliance Test icon opens a panel for selecting tests to be run.

Below the Compliance Test icon the Config Space icon opens for defining the Exerciser's PCIe configuration space parameters.

Always available at the bottom of the Exerciser window is the current test and bench status.

Xgig Analyzer User Interface

The Xgig PCIe 6.0 Analyzer/Exerciser user interface makes it easy to set up triggers, filters, trace depth, and start capturing PCIe traffic. The 6P16 hardware chassis and complementary Xgig software tools can support PCIe 6.0, CXL and NVMe.

The analyzer can be configured to alert the user to protocol errors at every layer of the PCIe stack including state and sub-state level errors within the LTSSM Viewer. Further, detection of FLIT packing, FEC, and CRC errors enable the user to get an accurate understanding of issues unique to the new PCIe 6.0 protocol.

The Xgig PCIe 6.0 Analyzer provides the foundation for deep protocol insights provided by the Xgig Expert tools. The transition from PCIe 5.0 to PCIe 6.0 brought significant changes at the protocol level, and with it the need for strong analysis tools to fully understand the protocol behavior. The combination of Xgig Analyzer and Expert provides the user incredible utility and flexibility in analyzing and debugging protocol issues.

The 6P16 Analyzer operates to 64GT/s and pairs with the new VIAVI series of function-specific Analyzer Interposers. The new PCIe 6.0 Interposers from VIAVI have been architected with a view to preserving signal integrity to limit impact on the link and provide the user a clear view of traffic on the link. The chassis and interposers are backward compatible with all other PCIe data rates.

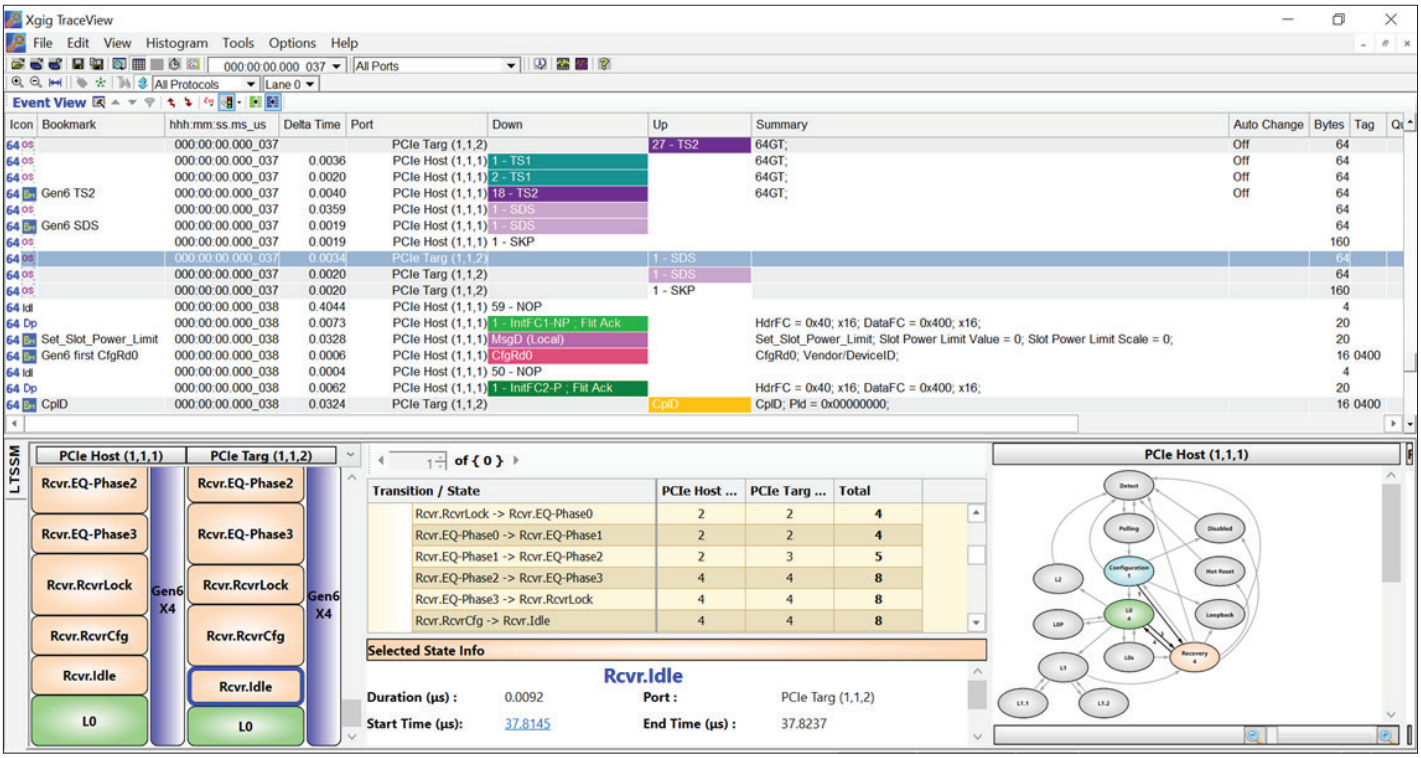

Figure 2 – PCIe6 Trace Capture with Xgig Analyzer

Test Applications

The following table lists some of the features available and tests that can be done using the Xgig PCIe Exerciser.

Support for new PCIe FLIT Mode	Define ROM write address space size and offset
Support for new PCIe FEC	Define Cfg read address space size and offset
Support for new TS0 Ordered Set	Define Mem64 read address space size and offset
Support for 64GT/s PCIe 6.0 PAM-4 signaling	Define Mem32 read address space size and offset
Control clock sources	Define IO read address space size and offset
Control and validate reset functions	Define ROM read address space size and offset
Control DUT power	Supports Config Space Type 0 Headers (32b)
LTSSM supported states: Detect, Quiet, Configuration, L0, L1, Recovery	Supports Config Space Type 1 Headers (64b)
Set data rate	Inject disparity errors option
Set link width	Inject symbol errors option
Edit LTSSM state transitions	Inject Sync Bit errors option
Control link width changes	Define ACK/NACK policies
Control link rate changes	Control ACK/NACK DLLP generation/reception
Test transitions: any speed/width to any other	Control idle generation
Control link state changes	Auto generate TLP sequence numbers
Set TX parameters	Auto generate TLP LCRC
Set RX parameters	Auto retransmit TLPs that NACK'd
Control equalization procedure	Validate state timeouts
Generates TLP 32b memory packets	Set replay timeouts
Generates TLP 64b memory packets	Control SKP generation
Generates TLP IO packets	Control over 8b/10b and 128b/130b encoding
Generates TLP configuration packets	Control and monitor sideband signals
Generates TLP message packets	Define custom test configurations, save and load
Execute bad TLP packets	Define custom test suites and execution sequence
Define TS0/TS1/TS2 data	View test description
Define Cfg write address space size and offset	View test results
Define Mem64 write address space size and offset	View LTSSM log
Define Mem32 write address space size and offset	View extensive error count information
Define IO write address space size and offset	

Ordering Information

Part Number	Description
XGIG6P-PCIE6-X16-PF	PCIe 6.0 16-Lane Analyzer/Exerciser Platform
XGIG6P-PCIE6-X16-AN	PCIe 6.0 16-Lane Analyzer License Key
XGIG6P-PCIE6-X16-EX	PCIe 6.0 16-Lane Exerciser License Key
XGIG6P-PCIE6-X16-AIC	PCIe 6.0 x16 Analyzer Interposer CEM
XGIG6P-PCIE6-X8-AIC	PCIe 6.0 x8 Analyzer Interposer CEM
XGIG6P-PCIE6-X16-AIED	PCIe 6.0 x16 Analyzer Interposer EDSFF
XGIG6P-PCIE6-X8-AIED	PCIe 6.0 x8 Analyzer Interposer EDSFF
XGIG6P-PCIE6-X16-EIC	PCIe 6.0 x16 Exerciser EP Interposer CEM
XGIG6P-PCIE6-X16-TSC	PCIe 6.0 x16 Host Exerciser Test Stand CEM
XGIG6P-PCIE6-X16-EIED	PCIe 6.0 x16 Exerciser EP Interposer EDSFF
XGIG6P-PCIE6-X16-TSED	PCIe 6.0 x16 Host Exerciser Test Stand EDSFF

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